

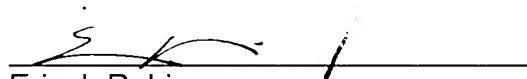
REMARKS

In response to the election requirement in the Office Action of January 13, 2003, Applicants hereby elect without traverse claims 5, 6, 9, 10, 11, and 13 and claims dependent thereon directed to signal line connections of a display device. Furthermore, it is respectfully submitted that at least claim 1 is generic to all species and thus subject to examination at this time.

Claims 5 and 6 have also been amended herewith to correct a minor typographical error.

Examination on the merits is requested.

Respectfully submitted,

A handwritten signature in dark ink, appearing to read 'Eric J. Robinson', is written over a horizontal line.

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend claims 5 and 6 as follows:

5. (Amended) A semiconductor device comprising:
a pixel portion comprising a plurality of pixels;
a signal line driver circuit; and
an output switching circuit,
wherein each of the plurality of pixels comprises a sensor portion and a light emitting element portion,
wherein the output switching circuit comprises a first logical circuit and a second logical circuit,
wherein a first signal line is connected to one of the first logical circuit and second logical circuit, and a second signal line is connected to the other,
wherein the signal line driver circuit outputs a timing [a] signal to the first logical circuit and to the second logical circuit,
wherein one of the first logical circuit and the second logical circuit outputs a first signal to the first signal line, and the other outputs a second signal to the second signal line, and
wherein the first signal is different from the second signal.
6. (Amended) A semiconductor device comprising:
a pixel portion comprising a plurality of pixels;
a signal line driver circuit; and
an output switching circuit,
wherein each of the plurality of pixels comprises a sensor portion and a liquid crystal element portion,
wherein the output switching circuit comprises a first logical circuit and a second logical circuit,
wherein a first signal line is connected to one of the first logical circuit and

wherein the signal line driver circuit outputs a timing [a] signal to the first logical circuit and to the second logical circuit,

wherein one of the first logical circuit and the second logical circuit outputs a first signal to the first signal line, and the other outputs a second signal to the second signal line, and

wherein the first signal is different from the second signal.